| CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): Dupuis et al. | | | Docket No. BUR920040106US1 |
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| Application No. 10/709,644 | Filing Date 5/19/2004 | Examiner Dang, Trung Q. | Group Art Unit 2823 |
| Invention: YIELD IMPROVEMENT IN SILICON-GERMANIUM EPITAXIAL GROWTH | | | |

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In Re Application Of: Dupuis et al.

| Application No. | Filing Date | Examiner | Customer No. | Group Art Unit | Confirmation No. |
|---|---|---|---|---|---|
| 10/709,644 | 5/19/2004 | Dang, Trung Q. | 30449 | 2823 | |

Invention: YIELD IMPROVEMENT IN SILICON-GERMANIUM EPITAXIAL GROWTH

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on 8/4/2005

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Docket No. BUR920040106US1

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Dupuis et al.

Group Art Unit: 2823

Filed: 05/19/2004

Examiner: Dang, Trung Q.

Serial No.: 10/709,644

Title: **YIELD IMPROVEMENT IN SILICON-GERMANIUM EPITAXIAL GROWTH**

Commissioner for Patents
P.O. Box 1450
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## BRIEF OF APPELLANT

This Appeal Brief, pursuant to the Notice of Appeal filed August 4, 2005, is an appeal from the rejection of the Examiner in the Office Action dated May 4, 2005.

## REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

## RELATED APPEALS AND INTERFERENCES

None.

## STATUS OF CLAIMS

Claims 1, 8-14, 21 and 33-35 are rejected. This Appeal Brief is in support of an appeal from the rejection of claims 1, 8-14, 21 and 33-35.



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PAGE 3/28 * RCVD AT 10/4/2005 12:08:02 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID: * DURATION (mm-ss):06-22

## STATUS OF AMENDMENTS

There are no After-Final Amendments which have not been entered.

## SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a method for forming semiconductor structures. A first plurality of identical semiconductor structures is formed, wherein each of the first plurality of identical semiconductor structures is formed as follows. See specification, paragraph [0027], lines 1-7.

A first step is to form a first region and a second region, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface. See specification, paragraph [0016], lines 7-16, and FIG. 1A.

A next step is to deposit a growth material simultaneously on top of the first and second regions so as to grow third and fourth regions from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface. See specification, paragraph [0018], lines 1-5, and FIG. 1C.

The first and third regions comprise a same material and have single-crystal atoms arrangement. See specification, FIG. 1C.

The first region has a different atoms arrangement than the fourth region. See specification, page 10, lines 3-7, and FIG. 1C, regions 120 and 150.

The step of depositing the growth material is performed under a first deposition condition. See specification, paragraph [0027], lines 3-7.

If a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, then a second plurality of identical semiconductor structures are formed. See specification, paragraph [0028], lines 1-6.

Each of the second plurality of identical semiconductor structures is formed using steps similar to the steps through which each of the first plurality of identical semiconductor structures is formed, except that the step of depositing the growth material is performed under a second deposition condition. See specification, paragraph [0028], lines 1-6.

If a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, then a third plurality of identical semiconductor structures may be formed. See specification, paragraph [0028], lines 17-24.

Each of the third plurality of identical semiconductor structures may be formed by using steps similar to the steps by which each of the first plurality of identical semiconductor structures is formed, except that the step of depositing the growth material is performed under a third deposition condition. See specification, paragraph [0028], lines 17-24.

The first, second, and third deposition conditions may comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, wherein $T1 < T2 < T3$. See specification, paragraph [0028], lines 5-6 and lines 21.

The first, second, and third deposition conditions may comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, wherein $P1 > P2 > P3$. See specification, paragraph [0029].

The first and second deposition conditions may comprise first and second temperatures, namely, T1 and T2, respectively, wherein $T1 < T2$. See specification, paragraph [0028], lines 5-6.

The first and second deposition conditions may comprise first and second pressures, namely, P1 and P2, respectively, wherein P1 > P2. See specification, paragraph [0029].

The first and second deposition conditions may comprise first and second precursor flow rates, namely, F1 and F2, respectively, wherein F1 > F2. See specification, paragraph [0029].

The first and third regions may comprise single-crystal silicon. See specification, page 10, lines 3-7, and FIG. 1C, regions 120 and 150.

The growth material may comprise silicon and germanium. See specification, paragraph [0018], lines 5-7.

The second region may comprise a dielectric material. See specification, paragraph [0016], lines 10-14, and FIG. 1C

The fourth region may comprise a polysilicon material. See specification, page 10, lines 3-7.

In forming each of the first plurality of identical semiconductor structures, another step may be performed to form a seed layer on top of the second region before the step of depositing the growth material. See specification, paragraph [0017], lines 1-3.

The seed layer may comprise a same material as the fourth region. See specification, paragraph [0017], lines 1-3, and page 10, lines 3-7.

The seed layer may be formed as follows. A first step is to deposit the seed layer on top of both the first and second regions. A next step is to remove a portion of the seed layer on top of the first region. See specification, page 9, lines 2-9.

The present invention also provides a method for forming semiconductor structures. A first plurality of identical semiconductor structures is formed, wherein each of the first plurality

of identical semiconductor structures is formed as follows. See specification, paragraph [0027], lines 1-7.

A first step is to form a first single-crystal semiconductor region and first and second shallow trench isolation regions on a semiconductor substrate, wherein the first single-crystal semiconductor region is sandwiched between the first and second shallow trench isolation regions. See specification, paragraph [0016], lines 7-16, and FIG. 1A.

A next step is to deposit a growth material simultaneously (A) on top of the first single-crystal semiconductor region to grow a second single-crystal semiconductor region from the first single-crystal semiconductor region and (B) on top of the first and second shallow trench isolation regions to grow first and second polysilicon regions from the first and second shallow trench isolation regions, respectively. See specification, paragraph [0018], lines 1-5, and FIG. 1C.

The second single-crystal semiconductor region and the first polysilicon region are in direct physical contact with each other. See specification, FIG. 1C.

The second single-crystal semiconductor region and the second polysilicon region are in direct physical contact with each other. See specification, FIG. 1C.

The step of depositing the growth material is performed under a first deposition condition. See specification, paragraph [0027], lines 3-7.

If a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, then a second plurality of identical semiconductor structures is formed. See specification, paragraph [0028], lines 1-6.

Each of the second plurality of identical semiconductor structures is formed using steps similar to the steps through which each of the first plurality of identical semiconductor structures

is formed, except that the step of depositing the growth material is performed under a second deposition condition. See specification, paragraph [0028], lines 1-6.

The present invention also provides a method for forming semiconductor structures. A first plurality of identical semiconductor structures is formed, wherein each of the first plurality of identical semiconductor structures is formed as follows. See specification, paragraph [0027], lines 1-7.

A first step is to provide a silicon substrate. See specification, paragraph [0016], lines 5-7.

Another step is to form a single-crystal silicon layer on the substrate. See specification, paragraph [0016], lines 7-10.

Yet another step is to form first and second shallow trench isolation regions in the single-crystal silicon region, the first and second shallow trench isolation regions defining a first single-crystal silicon region sandwiched between the first and second shallow trench isolation regions. See specification, paragraph [0016], lines 10-14.

Still yet another step is to grow a seed layer of polysilicon on top of the first and second shallow trench isolation regions. See specification, paragraph [0017], lines 1-3.

Still yet another step is to deposit silicon and germanium simultaneously (A) on top of the first single-crystal silicon region so as to grow a second single-crystal silicon region and (B) on top of the first and second shallow trench isolation regions so as to grow first and second polysilicon regions, respectively. See specification, paragraph [0018], lines 1-5, and FIG. 1C.

The second single-crystal silicon region and the first polysilicon region are in direct physical contact with each other. See specification, FIG. 1C.

The second single-crystal silicon region and the second ploy-silicon region are in direct physical contact with each other. See specification, FIG. 1C.

The step of depositing silicon and germanium is performed under a first deposition condition. See specification, paragraph [0027], lines 3-7.

If a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, then a second plurality of identical semiconductor structures is formed. See specification, paragraph [0028], lines 1-6.

Each of the second plurality of identical semiconductor structures is formed using steps similar to the steps through which each of the first plurality of identical semiconductor structures is formed, except that the step of depositing silicon and germanium is performed under a second deposition condition. See specification, paragraph [0028], lines 1-6.

The first yield of the first plurality of identical semiconductor structures is a function of a percentage of satisfactory structures of the first plurality of identical semiconductor structures in all the first plurality of identical semiconductor structures. See specification, paragraph [0027], lines 7-10.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 8-11, 14, 33, and 34 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Coolbaugh et al. (US 2002/0185708).

2. Claims 21 and 35 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Emons et al. (US 6,100,152).

3. Claims 1, 12 and 13 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Khater et al. (US 2004/0188797).

## ARGUMENT

### GROUND OF REJECTION 1

Claims 1, 8-11, 14, 33, and 34 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Coolbaugh et al. (US 2002/0185708).

Claim 1

Appellants respectfully contend that Coolbaugh does not anticipate claim 1, because Coolbaugh does not teach each and every feature of claim 1.

More specifically, Coolbaugh does not teach the step of "(b) if a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures...." of claim 1. Here, the step of "forming a second plurality of identical semiconductor structures" is a conditional step which is performed if the if condition in step (b) of claim 1 is satisfied. In contrast, Coolbaugh does not teach any conditional step based on a condition of a yield. In bullet number 2 of the non-final Office Action mailed on 12/01/2004, the Examiner alleges that "independent claims 1 and 14 recite an "if" condition, which include an option where the first yield of the first plurality of identical semiconductor structures is within a pre-specified range, leading to a second run to form a second plurality of identical semiconductor structures being not carried out. In this instant, the reference reads on every limitation of the claims." Appellants respectfully maintain that claim 1 does not explicitly or impliedly include the alleged step of not forming the second plurality of identical semiconductor structures if the first yield is within the pre-specified range.

In response to Appellants' arguments above, the Examiner alleges, in the final Office Action mailed on May 4, 2005, that "The Examiner agrees that Coolbaugh does not teach step

(b). However, as noted in the rejection, step (b) of claim 1 is not necessarily always carried out because of the "if" condition. Particularly, step (b) implies two alternatives: (1) If a first yield is not satisfied then forming a second plurality of identical semiconductor structure. (2) If a first yield is satisfied then the step of forming a second plurality of identical semiconductor structure is not necessarily."

From the Examiner's arguments above in the final Office Action, Appellants have the impression that the Examiner is trying to apply the Markush group argument to step (b) of claim 1. In other words, the Examiner alleges that step (b) of claim 1 comprises a Markush group of two small steps: step (1) and step (2) mentioned above, and that, because step (2) of the Markush group is anticipated by Coolbaugh, therefore the entire Markush group (i.e., step (b) of claim 1) is also anticipated by Coolbaugh.

Appellants agree that if an element of a Markush group is anticipated by a prior art reference, the entire Markush group is anticipated by the reference. However, as Appellants previously argued, step (b) of claim 1 does not explicitly or impliedly include the alleged step (2) mentioned above (i.e., the step of not forming the second plurality of identical semiconductor structures if the first yield is within the pre-specified range). In other words, claim 1 does not say anything about what happens if a first yield is within the pre-specified range. On this point, the Examiner states, in the final Office Action mailed on May 4, 2005, that "it is well settle that the claims have to be read in light of the specification in order to determine the scope of the invention. In this respect, paragraphs [0027]-[0028] of the specification clearly indicates such alternatives. In the case of 2), Coolbaugh 's reference reads on the claimed limitation as noted in the rejection." Appellants respectfully disagree. Contrary to the Examiner's belief, it is well-

settled by court decisions that the limitations in specification are not to be incorporated into claims, and that the scope of a claim must be construed from the language of the claim itself.

In addition, even if the step (b) of claim 1 includes the alleged step (2) mentioned above (which Appellants deny), the two steps (1) and (2) mentioned above do not comprise a Markush group.

To support Appellants' arguments, Appellants would like to give an example. Assume that an inventor invents an inverter having an input and an output, wherein the inverter (i) generates a 1 at its output if the inverter receives a 0 at its input and (ii) generates a 0 at its output if the inverter receives a 1 at its input. If the Markush group argument mentioned above could be used to reject claims, it would be impossible to claim the inverter invention. More specifically, whatever is claimed in the claim for the inverter, there would be an implied step for the inverter to do nothing (or not to do what it is supposed to do, i.e., inverting) if there is no signal applied to its input. This implied step of doing nothing would be easily anticipated by a prior art reference. As a result, the entire claim for the inverter would be anticipated by the reference. This line of rejection arguments would be unacceptable by a court. Therefore, Appellants urge that the Examiner not use such Markush group argument to reject claim 1.

Appellants also note the Examiner's argument that "However, as noted in the rejection, step (b) of claim 1 is not necessarily always carried out because of the "if" condition." This gives Appellants the impression that the Examiner is trying to say that the "if" condition of step (b) of claim 1 makes step (b) equivalent to nothing (i.e., not qualified as a limitation), leaving step (a) as claim 1's only limitation, and that because step (a) is anticipated by Coolbaugh, the entire claim 1 is anticipated by Coolbaugh. Appellants respectfully disagree. On the one hand, contrary to the

Examiner's belief, it is well-settled that a conditional step is in fact a limitation. On the other hand, as argued in the example of the inverter invention above, this line of rejection arguments would be unacceptable by a court because this line of rejection arguments would make it impossible to get a patent for almost anything. More specifically, this line of rejection arguments would infer that the inverting feature of the inverter in the example above is not a limitation just because the inverter does nothing if no signal is applied to its input. Without the inverting feature in the claim for the inverter, the claim for the inverter would be easily anticipated by prior art references. As a result, Appellants urge that the Examiner not reject claim 1 based on the argument that the "if" condition makes step (b) of claim 1 equivalent to nothing.

Based on the preceding arguments, Appellants respectfully maintain that Coolbaugh does not anticipate claim 1, and that claim 1 is in condition for allowance.

Claims 8-11

Since claims 8-11 depend from claim 1, which Appellants have argued *supra* to not be anticipated by Coolbaugh under 35 U.S.C. 102(b), Appellants contend that claims 8-11 are likewise not anticipated by Coolbaugh under 35 U.S.C. 102(b).

Claim 14

Based on similar arguments for claim 1 above, Appellants respectfully maintain that Coolbaugh does not anticipate claim 14, and that claim 14 is in condition for allowance.

Claims 33 and 34

Since claims 33 and 34 depend from claims 1 and 14, respectively, which Appellants have argued *supra* to not be anticipated by Coolbaugh under 35 U.S.C. 102(b), Appellants contend that claims 33 and 34 are likewise not anticipated by Coolbaugh under 35 U.S.C. 102(b).

**GROUND OF REJECTION 2**

Claims 21 and 35 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Emons et al. (US 6,100,152).

Claim 21

Based on similar arguments for claim 1 above, Appellants respectfully maintain that Emons does not anticipate claim 21, and that claim 21 is in condition for allowance.

Claim 35

Since claim 35 depends from claim 21, which Appellants have argued *supra* to not be anticipated by Emons under 35 U.S.C. 102(b), Appellants contend that claim 35 is likewise not anticipated by Emons under 35 U.S.C. 102(b).

**GROUND OF REJECTION 3**

Claims 1, 12 and 13 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Khater et al. (US 2004/0188797).

Claim 1

Based on similar arguments for claim 1 above (against ground of rejection 1), Appellants respectfully maintain that Khater does not anticipate claim 1, and that claim 1 is in condition for allowance.

Claims 12 and 13

Since claims 12 and 13 depend from claim 1, which Appellants have argued *supra* to not be anticipated by Khater under 35 U.S.C. 102(e), Appellants contend that claims 12 and 13 are likewise in condition for allowance.

## SUMMARY

In summary, Appellant respectfully requests reversal of the May 4, 2005 Office Action rejection of claims 1, 8-14, 21 and 33-35.

Respectfully submitted,

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Dated: October 4, 2005

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**Docket No. BUR920040106US1**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Dupuis et al. Group Art Unit: 2823

Filed: 05/19/2004 Examiner: Dang, Trung Q.

Serial No.: 10/709,644

Title: **YIELD IMPROVEMENT IN SILICON-GERMANIUM EPITAXIAL GROWTH**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**APPENDIX A - CLAIMS ON APPEAL**

1. A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first region and a second region, wherein the first region and the second region are in direct physical contact with each other via a first common interface surface, and

(ii) depositing a growth material simultaneously on top of the first and second regions so as to grow third and fourth regions from the first and second regions, respectively, such that a second common interface surface between the third and fourth region grows from the first common interface surface,

wherein the first and third regions comprise a same material and have single-crystal atoms arrangement,

wherein the first region has a different atoms arrangement than the fourth region, and

wherein the step of depositing the growth material is performed under a first deposition condition; and

(b) if a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures, wherein each of the second plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a second deposition condition.

2. The method of claim 1, further comprising the step of if a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, forming a third plurality of identical semiconductor structures, wherein each of the third plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a third deposition condition.

3. The method of claim 2, wherein the first, second, and third deposition conditions comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, and wherein $T1 < T2 < T3$.

4. The method of claim 2, wherein the first, second, and third deposition conditions comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, and wherein $P1 > P2 >$

P3.

5. The method of claim 1, wherein the first and second deposition conditions comprise first and second temperatures, namely, T1 and T2, respectively, and wherein T1 < T2.

6. The method of claim 1, wherein the first and second deposition conditions comprise first and second pressures, namely, P1 and P2, respectively, and wherein P1 > P2.

7. The method of claim 6, wherein the first and second deposition conditions comprise first and second precursor flow rates, namely, F1 and F2, respectively, and wherein F1 > F2.

8. The method of claim 1, wherein the first and third regions comprise single-crystal silicon.

9. The method of claim 1, wherein the growth material comprises silicon and germanium.

10. The method of claim 1, wherein the second region comprises a dielectric material.

11. The method of claim 1, wherein the fourth region comprises a polysilicon material.

12. The method of claim 1, further comprising the step of forming a seed layer on top of the second region before the step of depositing the growth material, whereas the seed layer comprises a same material as the fourth region.

13. The method of claim 12, wherein the step of forming the seed layer comprises the steps of:

depositing the seed layer on top of both the first and second regions; and

removing a portion of the seed layer on top of the first region.

14. A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) forming a first single-crystal semiconductor region and first and second shallow trench isolation regions on a semiconductor substrate, wherein the first single-crystal semiconductor region is sandwiched between the first and second shallow trench isolation regions, and

(ii) depositing a growth material simultaneously (A) on top of the first single-crystal semiconductor region to grow a second single-crystal semiconductor region from the first single-crystal semiconductor region and (B) on top of the first and second shallow trench isolation regions to grow first and second polysilicon regions from the first and second shallow trench isolation regions, respectively,

wherein the second single-crystal semiconductor region and the first polysilicon region are in direct physical contact with each other,

wherein the second single-crystal semiconductor region and the second polysilicon region are in direct physical contact with each other, and

wherein the step of depositing the growth material is performed under a first deposition condition; and

(b) if a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures, wherein each of the second plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a second deposition condition.

15. The method of claim 14, further comprising the step of if a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, forming a third plurality of identical semiconductor structures, wherein each of the third plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) and (a)(ii), except that the step of depositing the growth material is performed under a third deposition condition.

16. The method of claim 15, wherein the first, second, and third deposition conditions comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, and wherein $T1 < T2 < T3$.

17. The method of claim 15, wherein the first, second, and third deposition conditions comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, and wherein $P1 > P2 > P3$.

18. The method of claim 14, wherein the first and second deposition conditions comprise first

and second temperatures, namely, T1 and T2, respectively, and wherein T1 < T2.

19. The method of claim 14, wherein the first and second deposition conditions comprise first and second pressures, namely, P1 and P2, respectively, and wherein P1 > P2.

20. The method of claim 19, wherein the first and second deposition conditions comprise first and second precursor flow rates, namely, F1 and F2, respectively, and wherein F1 > F2.

21. A method for forming semiconductor structures, the method comprising the steps of:

(a) forming a first plurality of identical semiconductor structures, wherein each of the first plurality of identical semiconductor structures is formed by:

(i) providing a silicon substrate,

(ii) forming a single-crystal silicon layer on the substrate,

(iii) forming first and second shallow trench isolation regions in the single-crystal silicon region, the first and second shallow trench isolation regions defining a first single-crystal silicon region sandwiched between the first and second shallow trench isolation regions,

(iv) growing a seed layer of polysilicon on top of the first and second shallow trench isolation regions, and

(v) depositing silicon and germanium simultaneously (A) on top of the first single-crystal silicon region so as to grow a second single-crystal silicon region and (B) on top of the first and second shallow trench isolation regions so as to grow first and second polysilicon regions, respectively,

wherein the second single-crystal silicon region and the first polysilicon region are in direct physical contact with each other,

wherein the second single-crystal silicon region and the second ploy-silicon region are in direct physical contact with each other, and

wherein the step of depositing silicon and germanium is performed under a first deposition condition; and

(b) if a first yield of the first plurality of identical semiconductor structures is not within a pre-specified range of a target yield, forming a second plurality of identical semiconductor structures, wherein each of the second plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) through (a)(v) except that the step of depositing silicon and germanium is performed under a second deposition condition.

22. The method of claim 21, further comprising the step of if a second yield of the second plurality of identical semiconductor structures is not within the pre-specified range of the target yield, forming a third plurality of identical semiconductor structures, wherein each of the third plurality of identical semiconductor structures is formed by using steps similar to steps (a)(i) through (a)(v), except that the step of depositing silicon and germanium is performed under a third deposition condition.

23. The method of claim 22, wherein the first, second, and third deposition conditions comprise first, second, and third temperatures, namely, T1, T2, and T3, respectively, and wherein T1 < T2 < T3.

24. The method of claim 22, wherein the first, second, and third deposition conditions comprise first, second, and third pressures, namely, P1, P2, and P3, respectively, and wherein P1 > P2 > P3.

25. The method of claim 21, wherein the first and second deposition conditions comprise first and second temperatures, namely, T1 and T2, respectively, and wherein T1 < T2.

26. The method of claim 21, wherein the first and second deposition conditions comprise first and second pressures, namely, P1 and P2, respectively, and wherein P1 > P2.

27. The method of claim 26, wherein the first and second deposition conditions comprise first and second precursor flow rates, namely, F1 and F2, respectively, and wherein F1 > F2.

33. The method of claim 1, wherein the first yield of the first plurality of identical semiconductor structures is a function of a percentage of satisfactory structures of the first plurality of identical semiconductor structures in all the first plurality of identical semiconductor structures.

34. The method of claim 14, wherein the first yield of the first plurality of identical semiconductor structures is a function of a percentage of satisfactory structures of the first plurality of identical semiconductor structures in all the first plurality of identical semiconductor

structures.

35. The method of claim 21, wherein the first yield of the first plurality of identical semiconductor structures is a function of a percentage of satisfactory structures of the first plurality of identical semiconductor structures in all the first plurality of identical semiconductor structures.

**Docket No. BUR920040106US1**

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**APPENDIX B - EVIDENCE**

There is no evidence entered by the Examiner and relied upon by Appellant in this appeal.

**Docket No. BUR920040106US1**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Dupuis et al.

Group Art Unit: 2823

Filed: 05/19/2004

Examiner: Dang, Trung Q.

Serial No.: 10/709,644

Title: **YIELD IMPROVEMENT IN SILICON-GERMANIUM EPITAXIAL GROWTH**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**APPENDIX C - RELATED PROCEEDINGS**

There are no proceedings identified in the "Related Appeals and Interferences" section.